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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P8837 Total Pages 2

First Named Inventor or Application Identifier Douglas R. Parker

Express Mail Label No. EL431686837US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 20)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 4)

4. X Oath or Declaration (Total Pages 6)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

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ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__X__ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
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Our Reference: 042390.P8837 *Patent*

FUSE SENSE CIRCUIT

Inventors: Douglas R. Parker and Martin S.Denham

Respectfully submitted,

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Sharon Farnus
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(Signature of person mailing paper or fee) 6.30.00 (Date signed)

Serial/Patent No.: not yet assigned Filing/Issue Date: herewith
Client: Intel Corporation
Title: FUSE SENSE CIRCUIT

BSTZ File No.: 042390.P8837 Atty/Secty Initials: JCL:sef
Date Mailed: June 30, 2000 Docket Due Date: _____

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Attorney Docket: 042390.P8837

APPLICATION FOR UNITED STATES LETTERS OF PATENT

FOR

FUSE SENSE CIRCUIT

Inventors: **Douglas R. Parker; and**
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Sharon Farnus 6·30·00

Sharon E. Farnus Date

FUSE SENSE CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to the field of integrated circuit devices. More particularly, the invention relates to circuits for sensing the state of a fuse device.

Background Information

In many integrated circuits, fuses are used to store information, form connections, program elements for redundancy, store identification or other information, or trim analog circuits by adjusting the resistance of a current path. These functions are typically referred to as "programming" a fuse.

To determine whether a fuse has been programmed, circuits that sense the state of fuses ususally distinguish between programmed and unprogrammed fuses by detecting a change in the resistance of the fuse device from a low to a high value. Sometimes the difference in resistance between a programmed fuse and an unprogrammed fuse is so small that the resistance difference is difficult to detect. This is especially true for fuses with smaller geometries (*e.g.*, line widths and device sizes), whose resistances can be harder to control in the manufacturing process. Conversely, sometimes the difference in resistance between a programmed fuse and an unprogrammed fuse is so large that there is a wide range of programmed resistance values as compared to their unprogrammed resistance values. This can be the case for polysilicon fuses whose unprogrammed resistance can vary by several ohms while the programmed resistance can vary across hundreds of ohms.

To accommodate newer technologies, circuits that sense the state of fuses must be sufficiently sensitive to reliably detect small changes in resistance to accurately discern between unprogrammed and programmed fuses. Merely increasing the current in a fuse sensing circuit to increase sensitivity is not a viable approach. If the current through an unprogrammed fuse is not low enough during sensing, the unprogrammed fuse may be erroneously programmed.

Additionally, reduced supply voltages in newer technologies results in smaller signals. As a result, fuse sense circuits operating at the lower supply voltages may not have sufficient gain to ensure accurate sensing.

Other issues common to integrated circuits must also be considered when designing circuits that sense the state of fuses. For example, voltage and current characteristics of integrated circuits typically change as the ambient temperature changes. Integrated circuits also have natural mismatches among components.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally equivalent elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the reference number, in which:

Figure 1 is a schematic diagram of a prior art fuse sensing circuit;

Figure 2 is a schematic diagram of a fuse sense circuit with a fully matched gain stage according to an embodiment of the invention;

Figure 3 is a schematic diagram of an exemplar fuse sense circuit with a transistor matched gain stage according to an embodiment of the invention;

Figure 4 is a schematic diagram of an exemplar fuse sense circuit with a matched gain stage according to an embodiment of the invention; and

Figure 5 is a schematic diagram of an exemplar fuse sense circuit sensed differentially according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

A fuse sense circuit is described in detail herein. In the following description, numerous specific details are provided, such as particular currents, voltages, types of fuses, transistor types, and numbers of fuses to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, etc. In other instances, well-known structures or operations are not shown or described in detail to avoid obscuring aspects of various embodiments of the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrases "in one embodiment" or "in an

embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

Figure 1 shows an integrated circuit comprising a prior art fuse sense circuit 100. The fuse sense circuit 100 includes a fuse sense amplifier 102 and a complementary metal oxide semiconductor (CMOS) inverter 104. The fuse sense circuit 100 includes two branches 105 and 107, each with two resistances 114 and 116, respectively, two loads 106 and 108, respectively, and two current mirror devices 110 and 112, respectively. The two branches 105 and 107 are coupled to each other in a current mirror configuration. The fuse sense amplifier 102 is coupled to the CMOS inverter 104 via a current mirror output node 120. The fuse sense circuit 100 is coupled to a voltage 130 and a voltage 132.

The fuse sense circuit 100 senses the state of the resistances 114 and 116 to determine whether either fuse is programmed. A sense enable signal node 118 is available to receive a sense enable signal, which, when operational, causes the fuse sense circuit 100 to sense the state of the resistances 114 and 116.

During sensing operations, which is when the sense enable signal is asserted, current sinks or sources through the resistances 114 and 116, thereby degenerating the voltages of the current mirror devices 110 and 112. The current mirror output node 120 has a potential (or voltage) that increases or decreases based on the state of the resistances 114 and 116. As the resistance 116 increases relative to the resistance 114, the current through the resistance 116, the current mirror device 112, and the load 108 decreases and the potential at the current mirror output node 120 is pulled towards the

voltage 130. Conversely, as the resistance 116 decreases relative to the resistance 114, the current through the resistance 116, the current mirror device 112, and the load 108 increases and the potential at the current mirror output node 120 is pulled towards the voltage 132. The potential on the post amplifier output node 150 crosses the potential on the current mirror output node 120 at a voltage equal to the trip point of the CMOS inverter 104. This value is independent of whether or not the reference resistance 114 is equivalent to the sense resistance 116.

One limitation of the prior art fuse sense circuit 100 is that when the CMOS inverter 104 is used to interpret the potential at the current mirror output node 120 the result is a high sensitivity to process, voltage and temperature. For example, if the trip point for the CMOS inverter 104 is half the voltage 132, to make the potential at the current mirror output node 120 read a "1" across all conditions, the minimum value of the resistance 116 for a nominal value of the resistance 114 might be several times the value of the resistance 114.

Alternatively, it may be extremely difficult to make the potential at the current mirror output node 120 read other than a "0." This may be the case when the resistance 116 has a nominal value. In such a case, the resistance 116 may have a variety of values and the potential at the current mirror output node 120 still may read a "0."

Moreover, a small change in the CMOS inverter 104 trip point may dramatically influence the values of the resistances 114 and 116 that result in a current mirror output node 120 that is interpreted by the CMOS inverter 104 as a "1" or a "0".

Figure 2 illustrates an aspect of the invention that optimizes sensitivity to process, voltage and temperature using a single-ended post amplifier. Figure 2 illustrates an exemplar fuse sense circuit 200, which has a fully matched gain stage. The fuse sense circuits according to aspects of the invention also accommodate greater mismatch among components.

The fuse sense circuit 200 has a sense amplifier 202 and a post amplifier 204. The sense amplifier 202 includes a reference branch 205 coupled to a sense branch 207 in a current mirror configuration. The post amplifier 204 coupled to the sense amplifier 202 via a current mirror output node 220.

The fuse sense circuit 200 also includes a reference load 206, a sense load 208, and a post amplifier load 222. Each of the loads 206, 208, and 222 has its source coupled to the voltage 230 and its drain coupled to the drain of a reference current mirror device 210, the drain of a sense current mirror device 212, and the drain of a post amplifier device 226, respectively. The source of the current mirror device 210, the source of the current mirror device 212, and the source of the post amplifier device 226 each are coupled to one terminal of a reference resistance 214, a sense resistance 216, and a post amplifier resistance 224, respectively. The opposite terminals of the reference resistance 214, the sense resistance 216, and the post amplifier resistance 224 are coupled to the voltage 232. The reference current mirror device 210 and the sense current mirror device 212 are coupled together in a current mirror configuration. The fuse sense circuit 200 is coupled to a voltage 232, which may be referred to as V_{CC}, and to a voltage 230, which may be referred to as V_{SS}.

The reference resistance 214 and the sense resistance 216 can both be implemented using fuse elements. Alternatively, the sense resistance 216 can be a fuse element and the reference resistance 214 can be a reference resistor, or a series of fuse elements forming a reference resistor. The implementation depends on the implementation of the sense amplifier 202, and is well known. The current mirror devices 210 and 212, as well as the post amplifier device 226, can be well-known p-channel MOS (PMOS) devices. Alternatively, the current mirror devices 210 and 212, and the post amplifier device 226 can be well-known n-channel MOS (NMOS) devices.

A sense enable signal can be coupled into the sense amplifier 202 and the post amplifier 204 via a sense enable input node 260. More specifically, the reference branch 205 can receive the sense enable signal via the gate of a reference load 206, to the sense branch 207 via the gate of a sense load 208, and to the post amplifier 204 via the gate of a post amplifier load 224.

Typically, the reference branch 205 and the sense branch 207 are programmed, via a program "zero" input 217 and a program "one" input 219, respectively. When the sense enable signal is asserted, the output of the sense amplifier 202 generates a potential at the current mirror output node 220 and thereby is coupled to the post amplifier 204. If the reference branch 205 is programmed, the sense branch is un-programmed, and the sense enable signal is asserted, the post amplifier output node 250 indicates a logical "one." Conversely, if the reference branch 205 is un-programmed, the sense branch 207 is programmed, and the sense enable signal is asserted, the post amplifier output node 250 indicates a logical "zero." Programming the fuse sense circuit 200 is accomplished using any well-known technique.

The post amplifier 204 is a gain stage with a trip point which, during operation, sufficiently tracks the voltage on the current mirror output node 220. In the embodiment depicted in Figure 2, the post amplifier 204 is a scaled replica of the reference branch 205. This means that the devices in the post amplifier 204 are scaled to maintain the same ratio as similar devices in the reference branch 205, such that components in the post amplifier 204 each matches the components in the reference branch 205. For example, the post amplifier load 222, post amplifier resistance 224, and post amplifier device 226 each matches the reference load 206, the reference resistance 214, and the reference current mirror device 210, respectively.

An alternative embodiment includes the post amplifier 204 a scaled replica of the sense branch 207. Moreover, in one embodiment, the reference branch 205 and the sense branch 207 are identical.

Also, in an embodiment, the transistors in the reference branch 205 include multiple transistors in parallel "legged devices." In this embodiment, the scaled replica includes a subset of identical transistors of the reference branch 205.

Of course, multiple gain stages can be added to multiple sense branches for redundancy and single-ended sensing. From the description herein, persons of ordinary skill in the relevant art would understand how to implement such embodiments.

The fuse sense circuit 200 provides greater signal development than with prior art. Because the matched gain stage has a trip point that sufficiently tracks the

reference voltage or the voltage in the reference branch, sensitivity to process, voltage, and temperature is reduced. This reduction in sensitivity allows a much lower differential resistance (between the reference and sense branches) to be accurately detected, even when the sense amplifier is not ideal. The fuse sense circuit 200 thereby accommodates greater mismatch of components.

The fuse sense circuit 200 provides more gain than the prior art fuse sense circuit 100 when a subsequent CMOS inverter is added, *i.e.,* coupled to the post amplifier output node 250. The potential on the output of the added CMOS inverter would have a higher gain than the potential at the output of the CMOS inverter 104 (node 150). This embodiment also uses safe currents.

A further gain increase is accomplished by eliminating the post amplifier resistance 224. This is shown in Figure 3, which is an exemplar fuse sense circuit 300 with a transistor matched gain stage. Note that a post amplifier PMOS pull-up device 326 has its source tied to the voltage 232. When operating, the trip point of the post amplifier 304 sufficiently tracks the potential on the current mirror output node 320 as the trip point of the post amplifier 204 sufficiently tracks the potential on the current mirror output node 220. However, the potential on the post amplifier output node 350 has a gain higher than the potential on post amplifier output node 250. With no post amplifier resistance the trip point of the post amplifier 304 suffers only slightly.

In another embodiment, the post amplifier CMOS pull-up device 326 could be moved from exactly scaled to compensate for the removal of the resistance 224. However, in the spirit of the invention, the post amplifier 304 still sufficiently tracks.

Figure 4 shows an exemplar fuse sense circuit 400 with a matched gain stage. The fuse sense circuit 400 has a post amplifier device 426 with its source tied to the voltage and a post amplifier load 422 with its gate tied to the voltage 332 instead of a sense enable signal input node 260. This embodiment allows the post amplifier load 422 to pull down a post amplifier output node 450 when the sense amplifier 402 is powered down (*i.e.*, when the sense enable signal is de-asserted).

The exemplar embodiments depicted by the fuse sense circuits 200, 300, and 400 have a threshold-programmed resistance for varied voltages. The threshold post-burn resistance for a program "one" and a program "zero" has been moved. For the same post-burn resistance, the fuse sense circuits 200, 300, and 400 allow accurate sensing at a much lower supply voltage. This feature greatly reduces the threshold supply voltage for which the integrated circuit can be designed.

In an alternative embodiment, one aspect of the invention optimizes sensitivity to process, voltage and temperature using a post amplifier to interpret the potential at the current mirror output node 120 differentially. Figure 5 is a schematic diagram of a fuse sense circuit 500 according to an embodiment of the invention operated differentially. The fuse sense circuit 500 includes a sense amplifier 502 and a differential amplifier 504. The sense amplifier 502 includes a current mirror 510 and two resistances 514 and 516. A sense enable signal node 518 is available to receive a sense enable signal, which, when operational, causes the fuse sense circuit 500 to sense the state of the resistances 514 and 516. The sense amplifier 502 is coupled to the non-inverting input of the differential amplifier 504 at a current mirror output node 520 and to the inverting input of the differential amplifier 504 at a current mirror output node 522.

When the potential at the current mirror output node 520 is exactly equal to the drain voltage of the current mirror device 510 the differential amplifier 504 will trip. If the resistance 514 is programmed, the resistance 516 is un-programmed, and a sense enable signal (or enable signal) is asserted on the sense enable node 518, the differential amplifier output node 550 indicates a logical "one." Conversely, if the resistance 514 is un-programmed, the resistance 516 is programmed, and the sense enable signal is asserted on the sense enable node 518, the differential amplifier output node 550 indicates a logical "zero." For perfectly matched transistors, the differential amplifier 504 trips when the resistances 514 and 516 are equal to each other.

Examination of the fuse sense circuit 500 also reveals that at or near the differential amplifier 504 trip point, the voltage at the drain of current mirror device 510 does not vary significantly with changes in either of the resistances 514 and 516. Moreover, the trip point of the differential amplifier 504 behaves more like a reference voltage rather than a trip point. This indicates that a single-ended post amplifier, as described above, could perform substantially as well as the differential amplifier 504 if the trip point of the single-ended post amplifier sufficiently followed the voltage at the drain voltage of current mirror device 510.

Other example embodiments include implementations involving other single-ended fuse cells. Although many of the embodiments shown herein implement NMOS loads and PMOS current mirrors, the complement of the fuse sense circuits described herein, whose implementation would be readily recognized using the description herein, function in the same manner for fuse sense circuits that have PMOS loads and NMOS current mirrors.

The above description of illustrated embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. These modifications can be made to the invention in light of the above detailed description.

The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

first circuit branch;

second circuit branch, coupled to the first circuit branch in a current mirror configuration;

an amplifier, coupled to the second circuit branch, comprising a scaled replica of the first branch and an output node; and

an enable node coupled to the first circuit branch, the second circuit branch, and the post amplifier to indicate a first logical state at the output node if the first circuit branch is programmed and the second circuit branch is un-programmed and to indicate a second logical state at the output node if the first circuit branch is un-programmed and the second branch is programmed.

2. The apparatus of claim 1, further comprising:

first, second, and third resistances each having one terminal coupled to a first voltage;

first, second, and third current mirror devices, each having one terminal coupled to an opposite terminal of the first, second, and third resistances, respectively, the third current mirror device matching the first current mirror device, the first current mirror device coupled to the second current mirror device in a current mirror configuration; and

first, second, and third loads each having one terminal coupled to an opposite terminal of the first, second, and third current mirror devices, respectively, a second

terminal coupled to a second voltage, the third load matching the first load, and a third terminal coupled to the enable node.

3. The apparatus of claim 2, further comprising a second branch output node coupled to the second branch and the first branch current mirror, a second branch output node potential to decrease if the second resistance increases relative to the first resistance and to increase if the second resistance decreases relative to the first resistance, an output node potential being equivalent to the second branch output node potential if the second resistance is equivalent to the first resistance.

4. The apparatus of claim 2, the amplifier further comprising a trip point to sufficiently track a potential on the first current mirror device terminal coupled to the first resistance.

5. The apparatus of claim 2, the amplifier further comprising a trip point to sufficiently track a potential on the first current mirror device terminal coupled to the first resistance and to trip the amplifier if the first resistance is approximately equal to the second resistance.

6. The apparatus of claim 2, the amplifier further comprising a trip point to sufficiently track a potential on the first current mirror device terminal coupled to the first resistance and to trip the amplifier if the potential on the first current mirror device terminal coupled to the first resistance is approximately equal to the second branch output node potential.

7. The apparatus of claim 2, further comprising the output node potential to be equivalent to the second branch output node potential if the first resistance is approximately equal to the second resistance.

8. The apparatus of claim 2, the first, second, and third resistances each further comprising a fuse element.

9. The apparatus of claim 1, the first, second, and third current mirror devices each further comprising p-channel material.

10. A resistance sense circuit, comprising:

first circuit branch;

second circuit branch coupled to the first branch in a current mirror configuration;

an amplifier coupled to the second circuit branch, the amplifier comprising a load having it's gate coupled to a first voltage and it's source coupled to a second voltage, and an output node; and

an enable node coupled to the first circuit branch and the second circuit branch to turn the current mirror on to enable the resistance sense circuit to indicate a logical state at the output node if an enable signal is asserted on the enable node, the first circuit branch is un-programmed and the second circuit branch is programmed.

11. The resistance sense circuit of claim 10, the output node further to indicate a value approximately equal to the first voltage if the enable signal is asserted and to indicate a value approximately equal to the second voltage if the enable signal is de-asserted.

12. The resistance sense circuit of claim 10, the first resistance further comprising a resistor and the second resistance further comprising a fuse element.

13. The resistance sense circuit of claim 10, further comprising:

first input node coupled to the second circuit branch to program the second circuit branch with a first logical state; and

second input node coupled to the first circuit branch to program the first circuit branch with a second logical state.

14. The resistance sense circuit of claim 10, further comprising:

first resistance and second resistance each having one terminal coupled to a voltage;

first and second current mirror device each having one terminal coupled to an opposite terminal of the first and second resistance, respectively, the first current mirror device coupled to the second current mirror device in a current mirror configuration;

third current mirror device matching the first current mirror device, the third current mirror device having a gate coupled to a second circuit branch output node and a source coupled to the voltage; and

first and second load each having one terminal coupled to an opposite terminal of the first and second current mirror device, respectively.

15. The resistance sense circuit of claim 14, further comprising:

first input node coupled between the second current mirror device and the second resistance to program the second resistance with a first logical state; and

second input node coupled between the first current mirror device and the first resistance to program the first resistance with a second logical state.

16. An apparatus, comprising:

a sense amplifier;

a current mirror having a current mirror output node and a current mirror drain; and

a differential amplifier coupled to the sense amplifier via the current mirror output node, the differential amplifier to change states if a potential on the current mirror output node is approximately equal to a potential on the current mirror drain.

17. The apparatus of claim 16, further comprising first resistance and second resistance coupled to a current mirror source.

18. The apparatus of claim 16, further comprising first resistance and second resistance coupled to a current mirror source, the first and second resistances comprising p-channel material.

19. The apparatus of claim 16, further comprising:

first resistance coupled to a current mirror source;

second resistance coupled to the current mirror source; and

an enable node coupled to the current mirror drain to enable the differential amplifier to indicate a logical state at a differential amplifier output node if an enable signal is asserted on the enable node, the first circuit resistance is un-programmed and the second resistance is programmed.

20. The apparatus of claim 16,the differential amplifier further comprising a second current mirror output node coupled to an inverting input of the differential amplifier.

21. An apparatus, comprising:

an amplifier having an output node; and

a gain stage, coupled to the amplifier, having a trip point to track a potential on the output node.

22. The apparatus of claim 21, the amplifier comprising a sense branch coupled to a reference branch in a current mirror configuration.

23. The apparatus of claim 22, the gain stage comprising a scaled replica of the reference branch or the sense branch.

24. The apparatus of claim 22, further comprising first and second voltages each coupled to the amplifier and the gain stage.

FUSE SENSE CIRCUIT

ABSTRACT OF THE DISCLOSURE

A fuse sense circuit has a sense amplifier and a post amplifier (gain stage). The sense amplifier has a reference branch and one or more sense (or fuse) branches. The fuse sense circuit determines the state of the fuses using safe currents and provides much higher gain than prior art. The post amplifier is a scaled replica of the reference branch or one of the sense branches in that the devices in the post amplifier maintain the same ratio as similar devices in the reference branch, and components in the post amplifier each matches components in the reference branch. The sense amplifier output is interpreted by the post amplifier's matched gain stage and has a trip point that sufficiently tracks the reference voltage. The result is reduced process and voltage sensitivity, which allows lower differential fuse resistance to be accurately detected with a non-ideal sense amplifier. Multiple gain stages may be added to multiple sense branches for redundancy and single-ended sensing.

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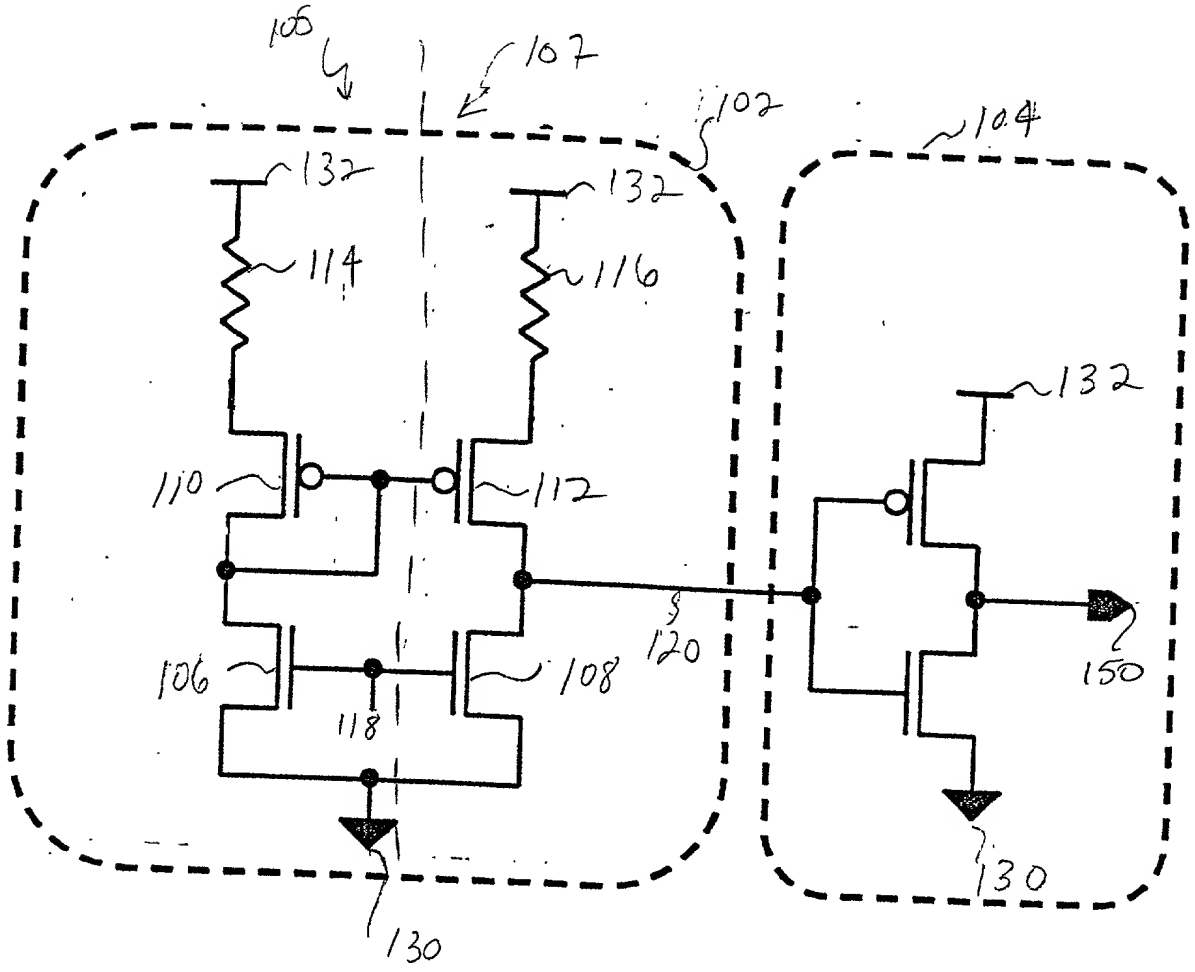
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Figure 1

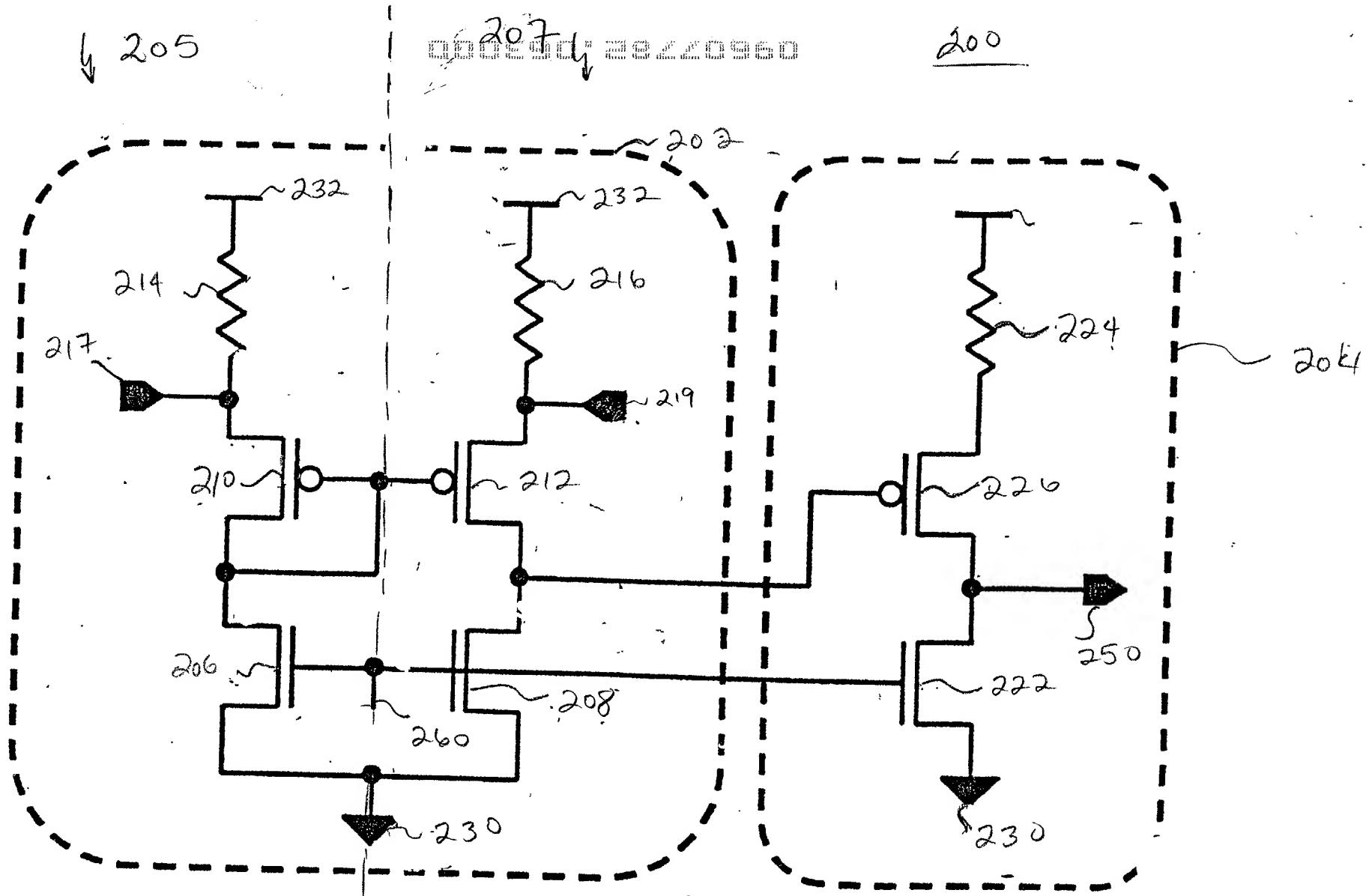
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Figure 2

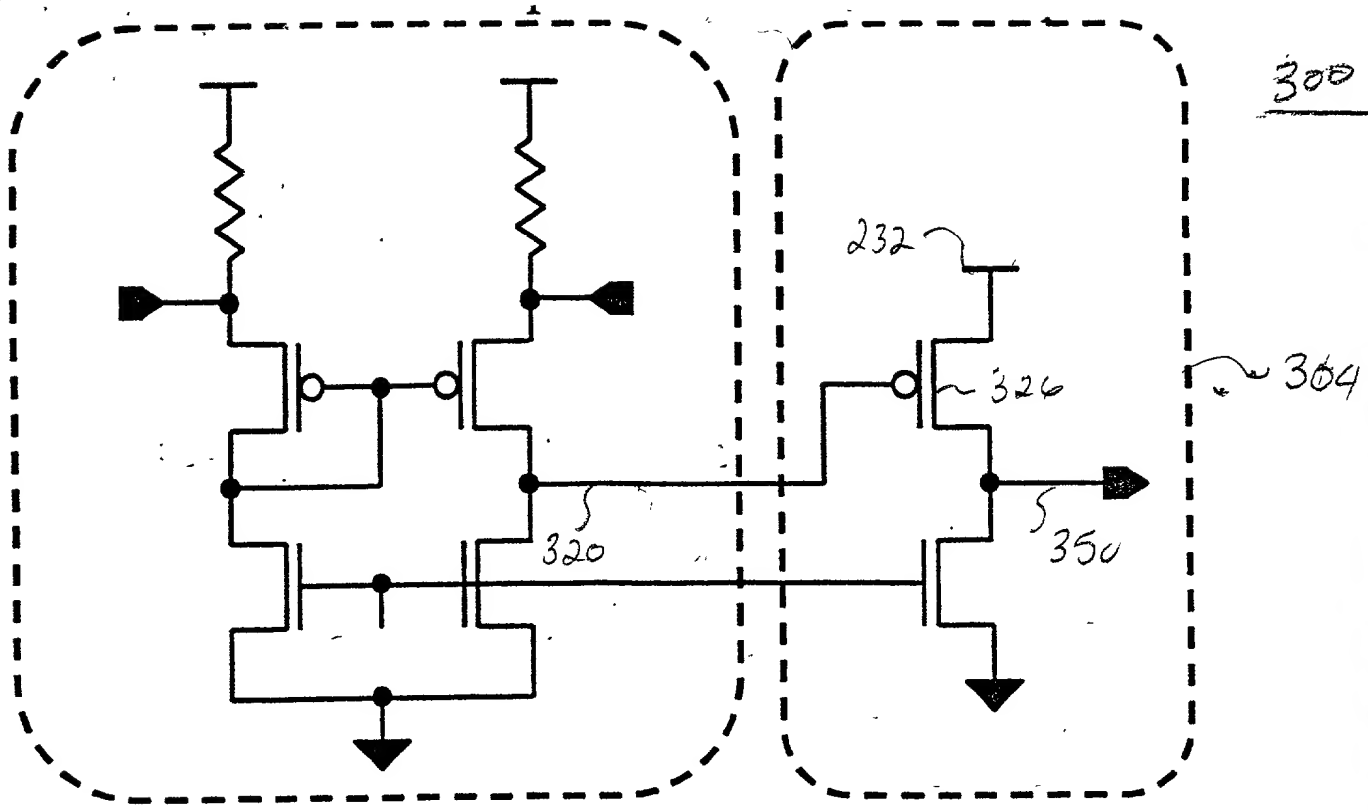

Figure 3

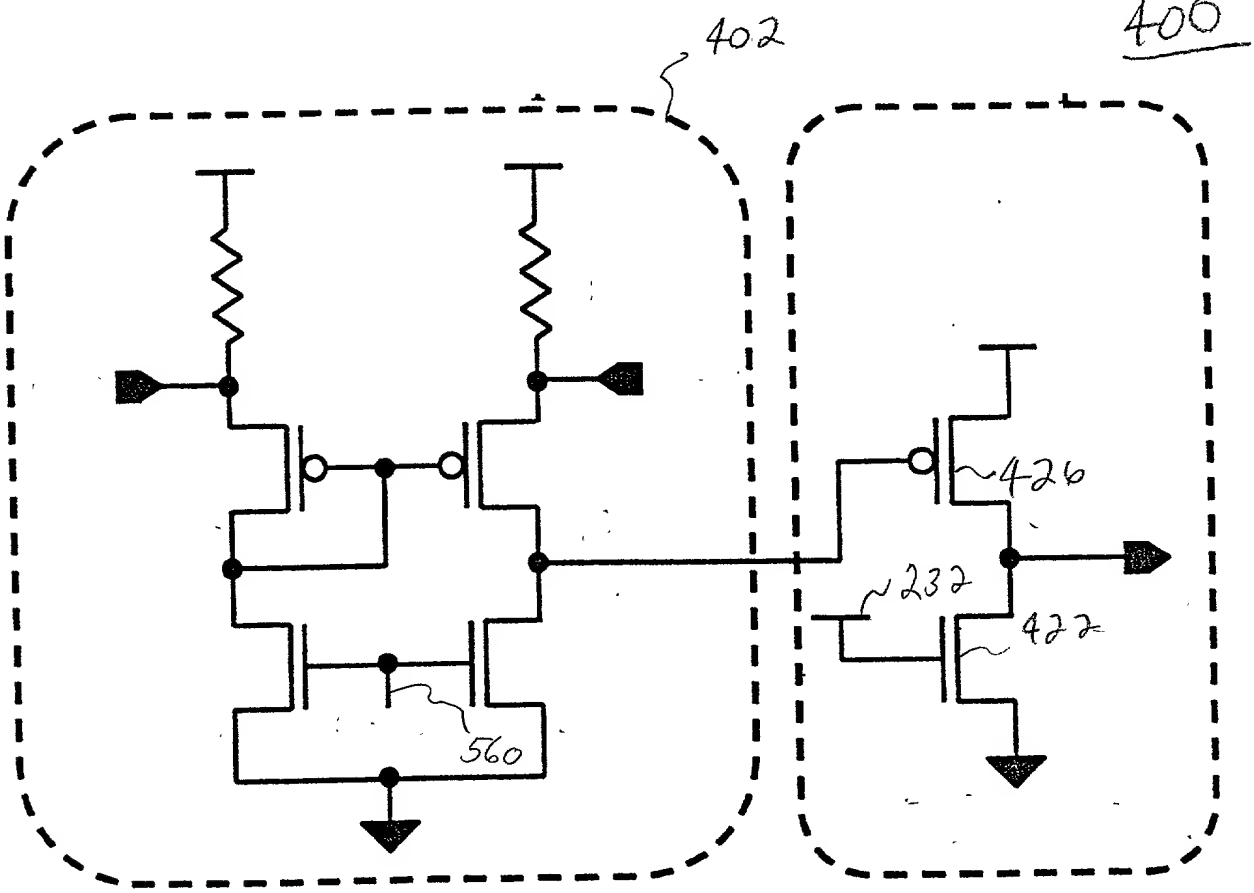

Figure 4

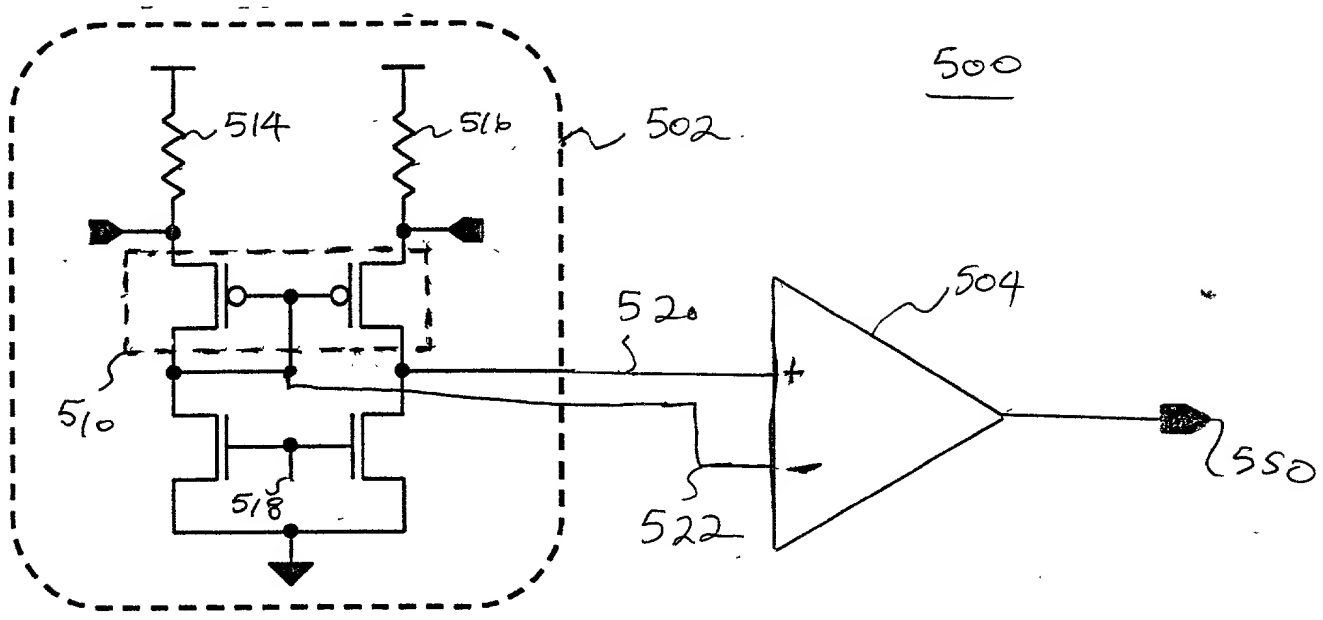

Figure 5

Attorney's Docket No.: 042390.P8837 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
FUSE SENSE CIRCUIT

the specification of which

XX is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Jan Carol Little, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Jan Carol Little, (425) 827-8600.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature ____________________ Date ____________

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Inventor's Signature ____________________ Date ____________

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Full Name of Third/Joint Inventor ____________________

Inventor's Signature ____________________ Date ____________

Residence ____________________ Citizenship ____________
(City, State) (Country)

Post Office Address ____________________

Full Name of Fourth/Joint Inventor ____________________

Inventor's Signature ____________________ Date ____________________

Residence ____________________ Citizenship ____________________
(City, State) (Country)

Post Office Address ____________________
____

Full Name of Fifth/Joint Inventor ____________________

Inventor's Signature ____________________ Date ____________________

Residence ____________________ Citizenship ____________________
(City, State) (Country)

Post Office Address ____________________
____

Full Name of Sixth/Joint Inventor ____________________

Inventor's Signature ____________________ Date ____________________

Residence ____________________ Citizenship ____________________
(City, State) (Country)

Post Office Address ____________________
____

Full Name of Seventh/Joint Inventor ____________________

Inventor's Signature ____________________ Date ____________________

Residence ____________________ Citizenship ____________________
(City, State) (Country)

Post Office Address ____________________
____

APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.